Remarks

In the non-final Office Action dated February 17, 2010, it is noted that the finality of the last Office Action has been withdrawn. The drawings remain objected to, and the following rejections are presented: claims 1-5 and 7-9 stand rejected under 35 U.S.C. § 103(a) over Yamada (U.S. Patent No. 5,757,639) in view of Stancil (U.S. Patent No. 6,272,584) and May (U.S. Patent No. 7,343,483); claim 6 stands rejected under 35 U.S.C. § 103(a) over the '639, '584 and '483 references in view of Sun Microelectronics (*Introduction to JTAG Boundary Scan*); claims 10-14 stand rejected under U.S.C. § 103(a) over the '639 and '584 references in view of Sun Microelectronics; claims 15-18 stand rejected under U.S.C. § 103(a) over the '639 and '584 references in view of Sun Microelectronics; and claims 15-18 stand rejected under U.S.C. § 103(a) over the '639 and '584 references further in view of Chang (U.S. Patent No. 6,484,273). In the following discussion, Applicant does not acquiesce in any regard to averments in this Office Action (unless Applicant expressly indicates otherwise).

Applicant traverses the § 103(a) rejections of claims 2 and 3 for lack of correspondence and, should the rejections be maintained, Applicant requests clarification of the rejections. The asserted combination of references lacks correspondence to certain claim limitations regarding using the test circuitry in a mode other than test mode. The Office Action cites to the '483 reference for these limitations, but the cited portions of the '483 reference do not teach such aspects. The rejections of claims 2 and 3 cite to column 13 of the '483 reference which does not exist. For at least this reason, and for the reasons stated below, the § 103(a) rejection of claims 2 and 3 is improper.

Applicant traverses the § 103(a) rejections of claims 1-9 because the Office Action has failed to provide a proper reason to combine the '639 reference, the '584 reference and the '483 reference to form the asserted hypothetical combination, contrary to the requirements § 2143.01. The Office Action on page 4 asserts that the motivation to combine the references would be "for the benefit of a test interface and the use of an industry standard protocol." However, the Office Action fails to explain what part of the '639 reference is being tested, or if the PLD controller of the '483 reference would be a proper testing protocol for the signal between the master CPU and the slave CPU of the '639 reference. Further, one of skill in the art would understand that CPUs of the '639

reference already include internal self-testing (software based) functionality as well as testing functionality from Figure 6 (step S4) and Figure 7 (stepS12). Also, CPUs are known to be testable by way of the functions they perform (*e.g.*, communications between the master and slave CPUs), and the serial line between the master and slave CPUs would not be tested by a PL-Device controller because it is not a programmable logic device. Moreover, the addition of a PLD controller as asserted would inherently increase the likelihood of the circuit not operating properly and require more testing of the device. Accordingly, the Office Action has failed to provide a proper reason for the proposed combination of references. The § 103(a) rejection of claims 1-9 must therefore be withdrawn.

Applicant further traverses the § 103(a) rejection of claims 1-9 because one of skill in the art would not be motivated to combine the references as claimed. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('639) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007). ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). Applicant submits that the combination would render the invention inoperable because "the master CPU checks whether or not the slave CPU is ready for serial reception in step 4." Col. 3:39-41. If the PLD controller was placed between the master and slave CPUs of the '639 reference, the master CPU would be unable to check whether the slave CPU was ready for serial reception. Under M.P.E.P. § 2143.01, the rejections cannot be maintained.

Further, the rejection of claims 1-9 has engaged in improper hindsight reconstruction. This hindsight reasoning is evidenced by the Office Action's statement at page 4 that "it would have been obvious to modify [the '639 reference] and [the '584 reference] to communicatively couple the first and second integrated circuits through test circuitry as taught by May for the benefit of a test interface to arrive at the invention as specified in the claims." Thus, the alleged motivation is "to arrive at Applicant's invention," which is *per se* improper. Under M.P.E.P. §2142, "impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts

gleaned from the prior art." As discussed above the Office Action has failed to provide a proper reason to combine the references. Further, the Office Action appears to acknowledge that the motivation to combine came from Applicant's claims. Accordingly, the § 103(a) rejection of claims 1-9 is improper and should be withdrawn.

Applicant traverses the § 103(a) rejections of claims 10-18 because the Office Action has failed to provide a proper reason to combine the '639 reference, the '584 reference and the Sun reference to form the asserted hypothetical combination, contrary to the requirements § 2143.01. The Office Action, on pages 9 and 12, asserts that the motivation to combine the references would be "for the benefit of a test interface and the use of an industry standard protocol." However, the Office Action fails to explain what part of the '639 reference is being tested or how the JTAG circuit of the Sun reference would (or could) be a proper testing protocol for the signal between the master CPU and the slave CPU of the '639 reference. Further, one of skill in the art would understand that CPUs of the '639 reference already include testing functionality from Figure 6 (step S4) and Figure 7 (stepS12). Also, the addition of a JTAG circuit as asserted would inherently increase the likelihood of the circuit not operating properly and require more testing of the device. Accordingly, the Office Action has failed to provide a proper reason for the proposed combination of references. The § 103(a) rejection of claims 10-18 must therefore be withdrawn.

Applicant further traverses the § 103(a) rejection of claims 10-18 because one of skill in the art would not be motivated to combine the references as claimed. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('639) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007). ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). Applicant submits that the combination would render the invention inoperable because "the master CPU checks whether or not the slave CPU is ready for serial reception in step 4." Col. 3:39-41. If the JTAG circuit was placed between the master and slave CPUs of the '639 reference, the master CPU would be

unable to check whether the slave CPU was ready for serial reception. Under M.P.E.P. § 2143.01, the rejections cannot be maintained.

Again, with this rejection of claims 10-18, the Office Action has engaged in improper hindsight reconstruction. This hindsight reasoning is evidenced by the Office Action's statements at pages 9 and 12 that "it would have been obvious to modify [the '639 reference] and [the '584 reference] to communicatively couple the first and second integrated circuits through test circuitry as taught by Sun Microelectronics for the benefit of a test interface to arrive at the invention as specified in the claims." Under M.P.E.P. §2142, "impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." As discussed above the Office Action has failed to provide a proper reason to combine the references. Further, the Office Action appears to acknowledge that the motivation to combine came from Applicant's claims. Accordingly, the § 103(a) rejection of claims 10-18 is improper and should be withdrawn.

Applicant further traverses the §103(a) rejection of claims 15-18 over the combination of the '639 reference and the '273 and '584 references because the Office Action has failed to provide a proper reason to combine the references as asserted in the hypothetical combination, contrary to the requirements of M.P.E.P. § 2143.01. The Office Action asserts the motivation would be "for the benefit of a non-intrusive development and debug technology". However, the Office Action again fails to provide any indication of what from the primary '639 reference is being tested, nor has the Office Action provided any explanation as to why master and slave CPUs coupled through a serial connection for the purposes outlined in the '639 reference require debugging. The Office Action fails to explain why an integrated JTAG is necessary when no bus is present, but rather a simple wire connecting the two CPUs. Accordingly, the § 103(a) rejection is improper and should be withdrawn.

Applicant further traverses the § 103(a) rejection of claims 15-18 over the combination of the '639 reference and the '273 and '584 references because the Office Action has engaged in improper hindsight reconstruction. This hindsight reasoning is evidenced by the Office Action's statement at page 15 that "it would have been obvious to modify [the '639 reference] and [the '584 reference] to implement a test circuit as taught by [the '273 reference] for the benefit of debugging technology to arrive at the

invention as specified in the claims." As discussed above, the alleged motivation is "to arrive at Applicant's invention," which is *per se* improper. Under M.P.E.P. §2142, "impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." As discussed above the Office Action has failed to provide a proper reason to combine the references. Further, the Office Action appears to acknowledge that the motivation to combine came from Applicant's claims. Accordingly, the § 103(a) rejection of claims 15-18 is improper and should be withdrawn.

In response to the objection to the drawings, Applicant submits that the objection is improper and not required under 37 C.F.R. 1.83(a). In support of Applicant's position reference is made to 35 USC §113 and M.P.E.P. § 601.01(f), which indicate that "applicant shall furnish a drawing *where necessary* for the understanding of the subject matter sought to be patented." The Office Action has not indicated why one skilled in the art would not be able to understand the claimed invention. In addition, M.P.E.P. § 601.01(f) indicates that it has been PTO practice to treat an application that contains at least one process or method claim as an application for which a drawing is not necessary for an understanding of the invention under 35 USC §113. Since most of the claims in the current application are method claims, Applicant has complied with M.P.E.P. § 601.01(f).

Notwithstanding M.P.E.P. § 601.01(f), Applicant submits that the claimed feature is adequately described by the reference to the numerical labels shown in Figures 4-8. For example, Figure 4 shows a high level schematic of a SoC, with testing circuitry 410 connected to bus 420. Further, the description of Figure 5 indicates that pathway 518 is connected to the test data output terminal of one SoC and test data input terminal of a second SoC. Accordingly the drawings depict IC circuits "communicatively coupled to one another through test circuitry that provides debugging capabilities, and transmitting, using the test circuitry, the second set of programming instructions." Office Action page 2. Therefore, Applicant requests the drawing objection be withdrawn.

In view of the above, Applicant believes that each of the rejections is improper and should be withdrawn and that the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, David Schaeffer, of NXP Corporation at (212) 876-6170 (or the undersigned).

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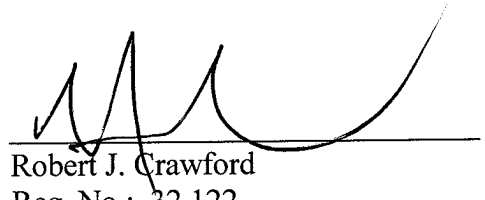
By: 

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